System-level Reliability Enhancement of DC/DC Stage in a Single-Phase PV Inverter

Peyghami, Saeed; Davari, Pooya; Wang, Huai; Blaabjerg, Frede

Published in:
Microelectronics Reliability

DOI (link to publication from Publisher):
10.1016/j.microrel.2018.07.112

Publication date:
2018

Document Version
Accepted author manuscript, peer reviewed version

System-level Reliability Enhancement of DC/DC Stage in a Single-Phase PV Inverter

Saeed Peyghami, Pooya Davari, Huai Wang, and Frede Blaabjerg
sap@et.aau.dk, pda@et.aau.dk, hwa@et.aau.dk, fbl@et.aau.dk

Department of Energy Technology, Aalborg University, Aalborg 9220 East, Denmark

Abstract

This paper studies the impact of modulation scheme, mission profile and PV array configuration on the reliability of a double-stage single-phase PV inverter. A single-phase double-stage inverter with two boost-based Maximum Power Point Tracker (MPPT) is considered and the reliability of dc/dc stage is estimated under different mission profiles. Furthermore, two types of PV panels with different output characteristics are considered to demonstrate the impact of PV array design on the PV converter reliability. Moreover, a phase shifted-switching scheme for the dc/dc converters and inverter is proposed to improve the overall reliability. The outcome is the PV converter reliability enhancement through suitable PV panel selection and proposed phase-shifted modulation scheme, which can be a system-level design for reliability guideline for PV converter and PV system designers.

1. Introduction

Power electronics plays a main role in energy conversion process of modern electronic power systems integrating renewable resources, electronic loads with the conventional power systems. Integrating power electronics in power systems is associated with many advantages including better controllability, flexibility, and efficiency. However, it is also pose to new challenges in terms of reliability and availability. Thermal cycling and power cycling are the main factors affecting the aging of active and passive components in a converter. These factors can trigger failure mechanisms of components, which should be managed during manufacturing, design, control and operation procedures.

Power module and capacitor manufacturers aim at improving the lifetime of power converters by strengthening individual components. Furthermore, improving the converter reliability can be feasible employing Design for Reliability (DfR) approaches during converter design procedure [1]–[3]. So far, mission profile based DfR methods have been presented to evaluate the converter reliability in order to maintain a desired lifetime.

Besides enhancing reliability at component and converter levels, the entire system reliability can be improved through active thermal management at control stage either by thermal stress reduction or thermal stress redistribution [4]. For instance, different modulation methods have been presented in order to reduce the thermal loss of converters in [5], [6]. Furthermore, reactive power injection under grid code requirements is presented in [7] in order to improve the temperature cycling of a wind turbine. Thermal stress reduction employing active power is further presented in [8], [9] by utilizing a storage system in the dc link of a back-to-back based wind converter. Lifetime extension by temperature swing reduction employing adjustable switching frequency is introduced in [4]. A power sharing approach is also presented in [10] in order to improve the reliability of parallel operated dc converters.

This paper proposes reliability enhancement approaches in a single-phase double-stage PV inverter in both system and control level. The main contribution of this paper is to illustrate the system-level impact of PV array characteristics on the converter reliability. Moreover, in the control level, a phase-shifted modulation scheme among different power stages is proposed, which can decrease the thermal losses and enhance the overall reliability.

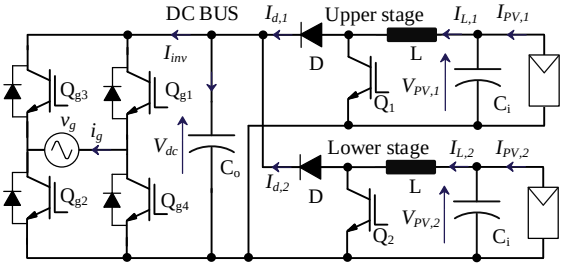

Fig. 1. Structure of the single-phase double-stage multiple MPPT PV inverter.

Table 1
Specifications of the PV Inverter.

Parameter	Symbol	Value
Rated Power of Inverter	*P (kW)*	5
Rated Power per MPPT	*P (kW)*	2.5
Boost Switching Frequency	f_{sw1} *(kHz)*	20
Inverter Switching Frequency	f_{sw2} *(kHz)*	10
DC Bus Voltage	V_{dc} *(V)*	400
AC Grid Voltage	V_g (V_{rms})	115
AC Grid Frequency	f_g *(Hz)*	50
Boost Inductor	L (mH)	2
Boost IGBT	*IKD06N60R*	
Boost Diode	*IDV15E65D2*	
DC Bus Capacitor (EPCOS)	*5×390 uF 450 V, 4.14 A*	
MPPT Algorithm	*Perturb & Observation*	

Table 2
Specifications of PV Panels.

Parameter	Symbol	Array I	Array II
Panel Rated Power	P_r (W)	320	320
Open Circuit Voltage	V_{oc} (V)	64.8	45.98
Short Circuit Current	I_{sc} (A)	6.24	8.89
MPPT Voltage	V_m (V)	54.7	36.73
MPPT Current	I_m (A)	5.86	8.58
Voltage temp. Coeff.	α (%/K)	-0.27	-0.33
Current temp. Coeff.	β (%/K)	0.056	0.058
Number of Series panels	N_s	4	8
Number of Parallel panels	N_p	2	1

2. PV System Structure

PV system includes two 2.5 kW PV arrays connected to the gird through a single-phase double-stage PV inverter with two boost-based MPPT as shown in Fig. 1 with the specifications summarized in Table 1. This inverter topology is used in SMA Sunny Boy 5000TL [11]. According to [11], the MPPT input voltage range of this converter is between 175 *V* to 440 *V*, and the maximum input voltage is 550 *V*. Therefore, any PV array configuration with the MPPT voltage staying in this region and the maximum open-circuit voltage lower than 550 *V*, can be connected to this type of inverters. In this study, two types of PV panels are considered: Array I with 2×4 PV panels, and Array II with 8 series connected PV panels. The rated power of each array is 2.5 kW, and the output power-voltage characteristics of arrays is shown in Fig. 2. The specifications of the PV arrays are summarized in Table 2. Furthermore, the PV system is modeled based on EN 50530:2010 [12] in order to fully consider the effect of solar Irradiance (I_{rr}) and ambient temperature (T_{amb}). The solar irradiance and ambient temperature data for two locations are used in this paper as shown in Fig. 3.

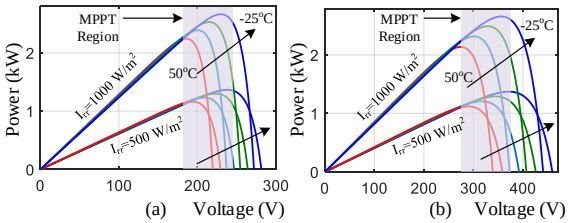

Fig. 2. Output characteristics of PV array configurations: (a) Array I (2×4 PV) and (b) Array II (1×8 PV).

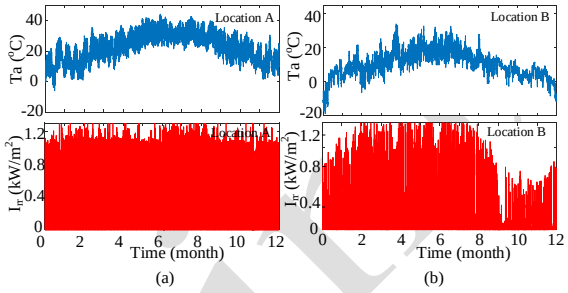

Fig. 3. Annual solar irradiance and ambient temperature for (a) location A, (b) Location B.

As it is seen in Fig. 3, the annual temperature of location A is higher than location B. Moreover, the annual solar irradiance in location A is higher than location B, hence the output power of PV system in both locations are different implying different converter loading for both mission profiles.

3. Reliability Prediction

The mission profile based reliability prediction method has been introduced in [2], [13], where, firstly an annual loading of the converter is translated to the converter components stress. The obtained stresses are compared to the component strength in order to find the corresponding failure rate and lifetime under given mission profile. Finally, the cumulative failure probability distribution function, also called unreliability function of the most fragile passive and active components in a power converter need to be predicted. The B_x lifetime of the converter is the time when its unreliability is equal to *x*% meaning that there is a x% possibility of converter failure after Bx lifetime operation.

The state-of-the-art lifetime model of electrolytic capacitors depends on the hot-spot temperature K_T, and operating voltage K_V, as:

$$L_{op} = L_r \cdot \underbrace{2^{\frac{T_r - T_{op}}{n_1}}}_{K_T} \underbrace{\left(\frac{V_{op}}{V_r}\right)^{-n_2}}_{K_V} \quad (1)$$

where L_r is the capacitor lifetime at a rated voltage V_r and a rated temperature T_r, and L_{op} is the capacitor lifetime at an operating voltage V_{op} and operating temperature T_{op}. The constant n_1 and n_2 are discussed in [14]. The accumulated damage of the capacitor

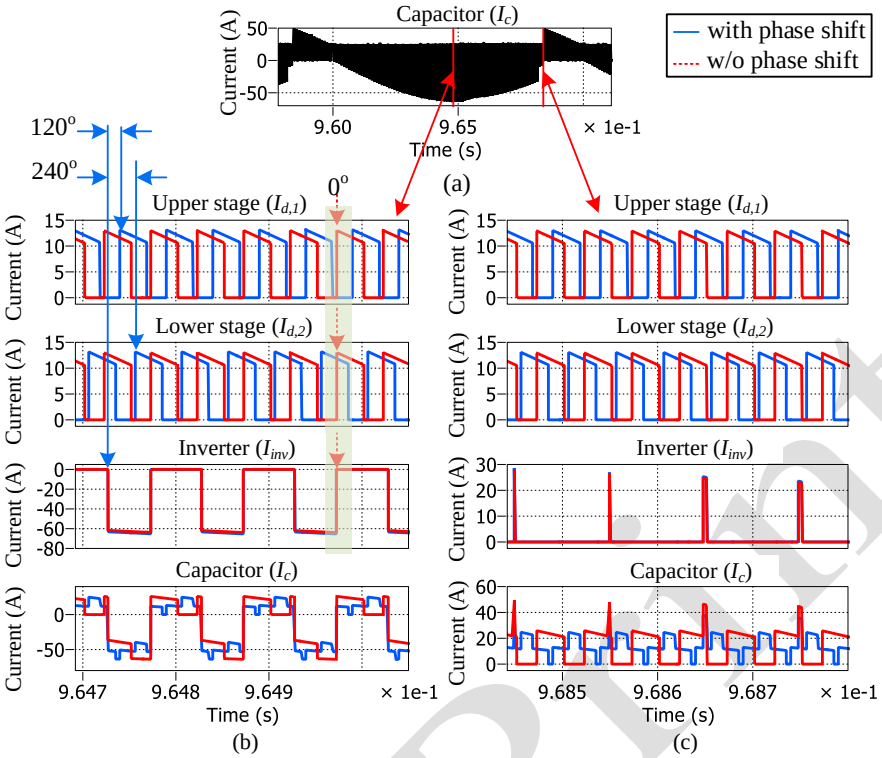

Fig. 4. Impact of high-frequency ripple elimination by phase shift: (a) capacitor bank current (b) converters current at peak current of capacitor, (c) converters current at zero crossing point of capacitor current.

can be found by $AD_c = \sum l_t/L_t$, where l_t is the time interval the capacitor stays under voltage V_t and hot-spot temperature T_t, and L_t is the lifetime of the capacitor under specific operating conditions following (1). The hot-spot temperature can be obtained by electro-thermal model of the capacitor as $T_t = T_{amb} + R_{th} \times P_{loss}$, where T_{amb} is the ambient temperature, R_{th} is the thermal resistance and P_{loss} is the power loss of the capacitor:

$$P_{loss} = ESR(100Hz)\cdot\left(I_{100Hz}^2 + \sum_f k_{ESR}(f)\cdot I_f^2\right)$$
$$k_{ESR}(f) = \frac{ESR(f)}{ESR(100Hz)} \quad (2)$$

$k_{ESR}(f)$ is given by the manufacturer. The capacitor lifetime hence can be obtained by the reliability data given in [11] for radial lead electrolytic capacitors with an upper category temprature of 105^oC and 5,000 h rated lifetime. Due to the higher ripple currents in dc link, a capacitor bank with five parallel connected capacitros is designed as reported in Table 1. Therefore, the reliaiblity of the capacitor bank including five capacitors connected in parallel can be found based on the series reliability network model.

Number of cycles to failure in Insulated Gate Bipolar Transistor (IGBT) switches and diodes depends on the junction temperature minimum value T_{jm}, temperature swing ΔT_j and heating time of power cycle t_{on} as given in (3), where the constants A, α and β are given in [2], [13].

$$N_f = A\cdot\Delta T_j^{\alpha}\cdot exp\left(\frac{\beta}{T_{jm}}\right)\cdot\left(\frac{t_{on}}{1.5}\right)^{-0.3},\ 0.1s \le t_{on} \le 60s \quad (3)$$

The accumulated damage of the IGBT switches is estimated by $AD_s = \sum n_f/N_f$, where n_f is the number of cycles with heating time t_{on}, T_{jm} and ΔT_j are minimum junction temperature and junction temperature swing induced by the mission profile respectively, and N_f is the number of cycles to failure under these loading condition which can be obtained by (3). Furthermore, Monte-Carlo simulation is employed to calculate the reliaibilty function of IGBTs following [2]. Moreover, the reliaiblity of the two IGBTs and two diodes of the two parallel-connected boost converters are found based on the series reliability network model.

4. Control System

The PV converter includes two boost units and a single-phase inverter as shown in Fig. 1. The control block diagram of the converters is shown in Fig. 5, where conventionally, the boost converters are working in MPPT mode and independent from the inverter control system, which is responsible for injecting the PV power into the grid and regulating the dc bus voltage. The high frequency ripple

currents of the converters are absorbed by the dc link capacitor bank, where boost converters introduce a 20 kHz ripple current and its harmonics. Furthermore, the inverter injects a 10 kHz ripple current and its harmonics as well as 100 Hz ripple current. According to the KCL at dc bus, the high frequency ripple currents can be reduced by making a phase shift among PWM carrier signals of the three converters. For instance, a 120° phase shift can reduce the 20 kHz ripple current of capacitor bank by 43% as shown in Fig. 4. Thereby, following (2), the power loss and consequently the hot-spot temperature of the capacitor bank is reduced and consequently the reliability is improved.

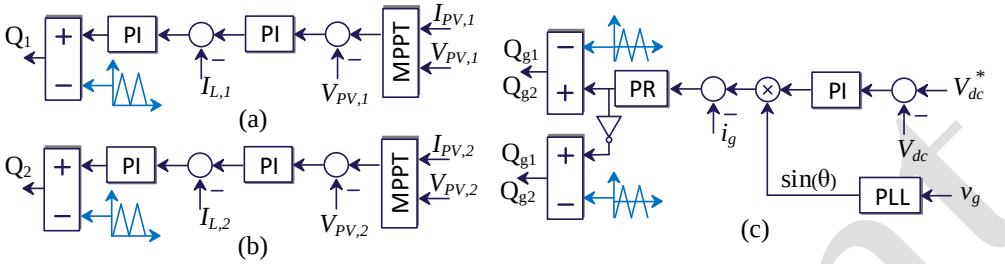

Fig. 5. Control block diagram of (a) upper DC/DC stage, (b) lower DC/DC stage, and (c) inverter.

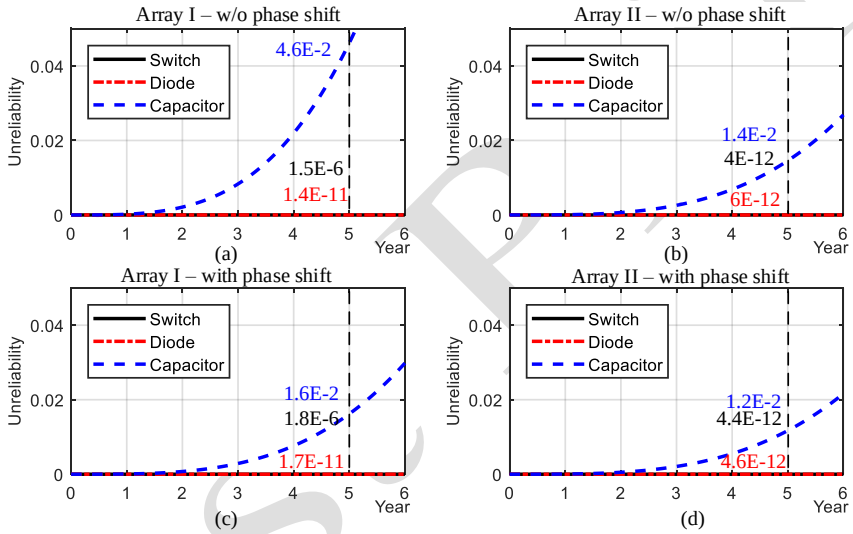

Fig. 6. Unreliability function of different components under mission profile A; (a) Array I w/o phase shift, (b) Array II w/o phase shift, (c) Array I with phase shift and (d) Array II with phase shift.

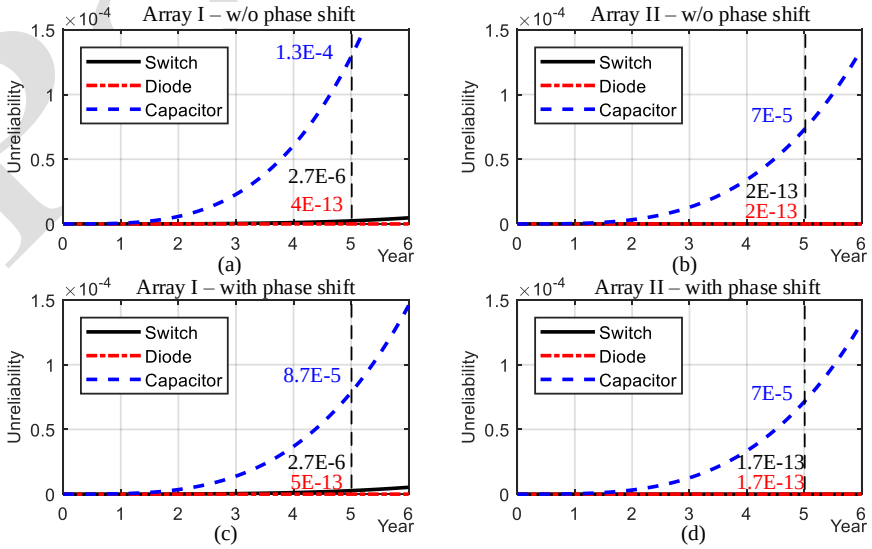

Fig. 7. Unreliability function of different components under mission profile B; (a) Array I w/o phase shift, (b) Array II w/o phase shift, (c) Array I with phase shift and (d) Array II with phase shift.

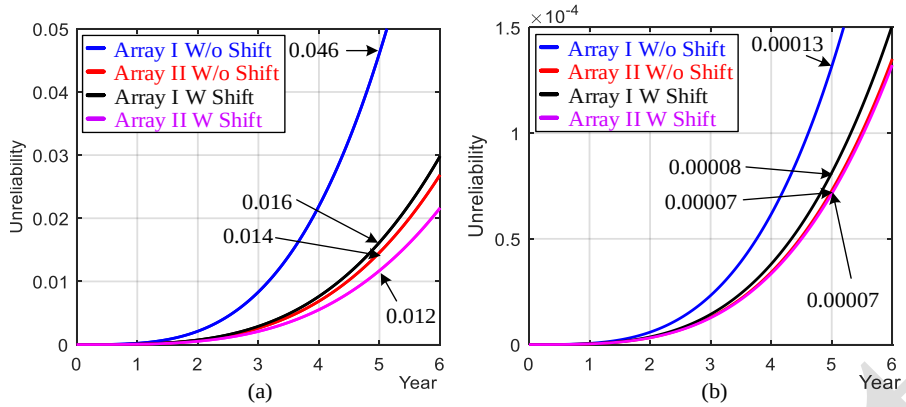

Fig. 8. Total Unreliability of converter under different case studies considering (a) mission profile A and (b) mission profile B.

5. Results and discussion

The cumulative distribution function of the failure probability, i.e., the unreliability function of dc/dc conversion stage of the PV converter is investigated under different PV array configurations, mission profiles and modulation schemes, and the obtained results are reported in Fig. 6 to Fig. 8. Fig. 6 and Fig. 7 show the unreliability of the converter components under mission profile A and B, respectively. Furthermore, the total unreliability of converter under mission profile A and B is illustrated in Fig. 8(a) and (b). The obtained results are summarized as follows:

(1) The dc link capacitor bank is the most fragile component of the converter as shown in Fig. 6 and Fig. 7. The dc link capacitor is affected by the low-frequency ripple currents induced by the single-phase inverter and high-frequency switching ripple currents, while very low frequency solar irradiance fluctuations are passing through the active switches (IGBTs and Diodes). Therefore, the unreliability of capacitor bank is higher than active switches.

(2) According to Fig. 6 and Fig. 7, the PV Array II has better reliability compared to the Array I under both mission profiles. According to Fig. 2, the MPPT voltage range for Array II is between 280 *V* and 380 *V*, while the MPPT voltage range of Array I is from 180 *V* to 250 *V*. Therefore, the duty cycle of boost converters in case of Array II is lower than Array I. The output ripple current of a boost converter I_{ripple} is

$$\frac{I_{ripple}}{I_o} \simeq \sqrt{\frac{D}{1-D}} \tag{4}$$

where I_o is the output dc current and D is the switching duty cycle. By increasing the duty cycle as shown in Fig. 9, the output ripple current will be increased. This ripple current is absorbed by the dc link capacitors. Hence, lower duty cycle introduces lower power loss and higher lifetime. Moreover, according to (5) [15] (the parameters' definition is given in page 276-277 in [15] – k_{T1}, k_{T2}, k_{T3}, and k_{T4} are the temperature coefficients, for IGBT k_i = 1, k_v = 1.3~1.4, and for diode k_i = k_v = 0.6), the IGBT and Diode switching and conduction power losses (P_{sw} and P_{cond}) will be reduced under lower duty cycle and lower input current I_{in} operation, consequently implying better reliability. Notably, for the both PV Arrays the output power and voltage of the converter is the same and increasing the input voltage will decrease the input current and switching duty cycle.

$$\begin{aligned}
P_{cond}(IGBT) &= (I_{in}\cdot(V_{ce0}+k_{T1}\cdot(T_j-25))) \\
&\quad + I_{in}^2\cdot(r_{ce}+k_{T2}\cdot(T_j-25))\cdot D \\
P_{cond}(Diode) &= (I_{in}\cdot(V_F+k_{T1}\cdot(T_j-25))) \\
&\quad + \frac{I_o^2}{1-D}\cdot(r_F+k_{T2}\cdot(T_j-25)) \\
P_{sw}(IGBT) &= f_{sw}\cdot E_{on+off}\cdot\left(\frac{I_{in}}{I_{ref}}\right)^{K_i}\cdot\left(\frac{V_o}{V_{ref}}\right)^{K_v} \\
&\quad \cdot(1+k_{T3}\cdot(T_j-T_{ref})) \\
P_{sw}(Diode) &= f_{sw}\cdot E_{rr}\cdot\left(\frac{I_{in}}{I_{ref}}\right)^{K_i}\cdot\left(\frac{V_o}{V_{ref}}\right)^{K_v} \\
&\quad \cdot(1+k_{T4}\cdot(T_j-T_{ref}))
\end{aligned} \tag{5}$$

Therefore, employing Array II decreases the power loss on the converter components and improves the reliability. As it is shown in Fig. 8(a), the unreliability of the converter is reduced from 4.6E-2 for the PV Array I to 1.4E-2 for the PV Array II during 5-year of converter lifetime, which means the failure probability is decreased by factor of 3 employing the PV Array I under mission profile A. Moreover, as shown in Fig. 8(b), employing Array II decreases the unreliability from 1.3E-4 to 7E-5 under mission profile B, and hence, the failure probability is decreased by factor of 2. Therefore, a proper design for PV Array collection can improve the

overall lifetime of the converter.

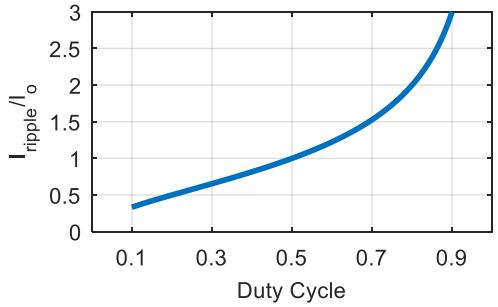

Fig. 9. Ripple current of a boost converter (I_{ripple}) in terms of switching duty cycle – I_o = output dc current.

(3) The dc link capacitor bank reliability is affected by the low- and high-frequency ripple currents. The high-frequency ripples are induced by the dc converters and inverter. Applying a suitable phase shift among switching carrier signal of converters, the high-frequency ripples can be eliminated. For instance, a 120° phase shift among the switching signals of converters can reduce the 20 kHz ripple current by 43% as shown in Fig. 4. Hence, the power loss and hot-spot temperature of capacitors can be decreased consequently improving the capacitor bank lifetime and reliability. The effect of phase shifted switching scheme on the reliability of components can be seen from Fig. 6(c, d) and Fig. 7(c, d). For instance, applying phase shifted scheme for the PV system with Array I under mission profile A, the unreliability of capacitor bank during its 5-year lifetime is decreased from 4.6E-2 to 1.6E-2 as shown in Fig. 6(a) and (c).

(4) The impact of location on the reliability of converter is illustrated in Fig. 8 for mission profile A and B. The unreliability of the converter under mission profile A is higher than the mission profile B during 5-year lifetime of the converter. According to Fig. 3, the annual solar irradiance in location A is higher than location B, and hence, the converted energy and annual converter loading in case of mission profile A is greater (≈ 20%) than mission profile B. Furthermore, the annual ambient temperature in location A is higher than location B, consequently, the thermal stress induced by mission profile A is greater than mission profile B.

6. Conclusion

This paper studies the influence of mission profile, PV panel configuration and phase-shifted modulation scheme on the reliability of a single-phase double-stage PV inverter system. According to the obtained results, the mission profile has dominant impact on the reliability of PV converters due to the thermal stresses on the converter components induced by the mission profile. Furthermore, an appropriate PV array collection design can considerably improve the PV converter reliability, since the output characteristics of the PV array determines the operating point of converter. A suitable coordination between control systems of converters can also reduce the dc link capacitor bank power loss and its hot-spot temperature, consequently improving the reliability of the converter. The mission profile-based numerical analysis validates the effectiveness of the PV array configuration design and proposed phase shifted switching scheme on the reliability of the single-phase double-stage PV inverter.

References

[1] H. Wang, K. Ma, and F. Blaabjerg, "Design for Reliability of Power Electronic Systems," in *Proc. IEEE IECON*, 2012, pp. 33–44.

[2] D. Zhou, H. Wang, and F. Blaabjerg, "Mission Profile Based System-Level Reliability Analysis of DC/DC Converters for a Backup Power Application," *IEEE Trans. Power Electron.*, p. Early Access, 2018.

[3] S. Peyghami, P. Davari, H. Wang, and F. Blaabjerg, "The Impact of Topology and Mission Profile on the Reliability of Boost-Type Converters in PV Applications," in *Proc. IEEE COMPEL*, 2018, pp. 1–8.

[4] M. Andresen, G. Buticchi, and M. Liserre, "Study of Reliability-Efficiency Tradeoff of Active Thermal Control for Power Electronic Systems," *Microelectron. Reliab.*, vol. 58, pp. 119–125, Mar. 2016.

[5] K. Ma and F. Blaabjerg, "Modulation Methods for Neutral-Point-Clamped Wind Power Converter Achieving Loss and Thermal Redistribution Under Low-Voltage Ride-Through," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 835–845, Feb. 2014.

[6] Y. Wu, M. A. Shafi, A. M. Knight, and R. A. McMahon, "Comparison of the Effects of Continuous and Discontinuous PWM Schemes on Power Losses of Voltage-Sourced Inverters for Induction Motor Drives," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 182–191, Jan. 2011.

[7] K. Ma, M. Liserre, and F. Blaabjerg, "Reactive Power Influence on the Thermal Cycling of Multi-MW Wind Power Inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 922–930, Mar. 2013.

[8] Z. Qin, M. Liserre, F. Blaabjerg, and H. Wang, "Energy Storage System by Means of Improved Thermal Performance of a 3 MW Grid Side Wind Power Converter," in *Proc. IEEE IECON*, 2013, pp. 736–742.

[9] Z. Qin, M. Liserre, F. Blaabjerg, and Poh Chiang Loh, "Reliability-Oriented Energy Storage Sizing in Wind Power Systems," in *Proc. IEEE IPEC*, 2014, pp. 857–862.

[10] S. Peyghami, P. Davari, and F. Blaabjerg, "System-Level Lifetime-Oriented Power Sharing Control of Paralleled DC/DC Converters," in *Proc. IEEE APEC*, 2018, pp. 1890–1895.

[11] SMA, "Sunny Boy 3000TL / 4000TL / 5000TL." [Online]. Available: http://files.sma.de/dl/5692/SB5000TL-DEN110731W.pdf. [Accessed: 12-May-2018].

[12] EN 50530:2010 + A1:2013, "Overall Efficiency of Grid Connected Photovoltaic Inverters," 2013.

[13] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of Bond Wire Fatigue of IGBTs in a PV Inverter under a Long-Term Operation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 3052–3059, Mar. 2016.

[14] A. Albertsen, "Electrolytic Capacitor Lifetime Estimation," *JIANGHAI Eur. GmbH*, pp. 1–13, 2010.

[15] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, "*Application Manual Power Semiconductors*," 2nd ed. Germany: ISLE Verlag, 2015.